

ECE321 – Electronics I

Lecture 1: Introduction to Digital Electronics

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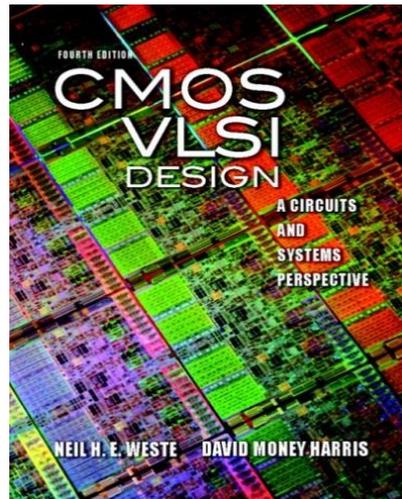
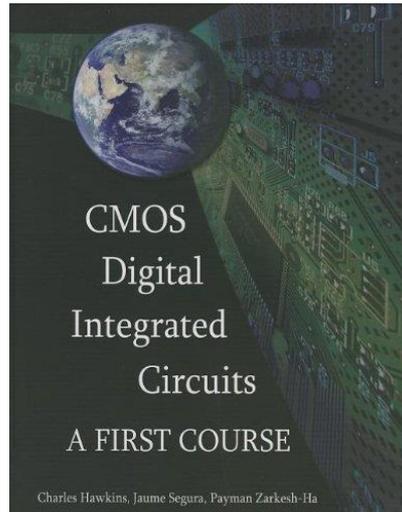
Textbook and Background

- ❑ **Main reference material is your notes in the class and the handouts**

- ❑ **Two equally important textbooks are:**
 - **Charles Hawkins, Jaume Segura, and Payman Zarkesh-Ha, "CMOS Digital Integrated Circuits: A First Course," SciTech Publishing, December 15, 2012, ISBN: 978-1613530023**
 - **Neil Weste and David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective," 4th Edition, Addison Wesley, March 11, 2010, ISBN-13: 978-0321547743**

- ❑ **Lecture Notes: combination of slides, homework and announcements**
 - **Slides will be posted on the class webpage**
 - **Class webpage: www.unm.edu/~pzarkesh/ECE321**

Textbooks and Outline



- **Basic CMOS Transistor Modeling**
- **CMOS Inverter**
- **Delay and Power Calculations**
- **Interconnect Modeling**
- **Design Rules and Layout**
- **Design Tools**
- **CMOS Fabrication**
- **Combinational / Sequential Logic**
- **Static / Dynamic / Domino Logic**
- **Basic Timing Analysis**
- **Basic SRAM and DRAM Memories**

Grading Policy

- Your grade in the course will be comprised of:**
 - Homework (20%)
 - Class Contribution (5%)
 - Design Project (15%)
 - Tests (30%)
 - Final Exam (30%)

- There will be 2 midterm tests, but only 1 will be considered and the worst test will be ignored. Therefore, there is no makeup tests or exams.**

- Final letter grade will be based on curve and class performance**

- Your participation in class is very important**

- Suggestions for success:**
 - Participate in the class and ask questions
 - Read the textbook
 - Work on problems

Homework Policy

- Homework will be assigned for each Monday of the class. Please refer to the class website for the homework assignments.
- Homework due at the beginning of the lecture. No exception!
- Solutions will be posted on the class website as soon as it is available.
- Late homework and projects will not be accepted

Course Project

- ❑ There will be design project assigned including:
 - Layout design using L-Edit
 - Circuit extract and spice simulation
- ❑ The design problem will be a team project. However, the roles of each team member should be rotated during the course of the project.
- ❑ Project grade will be based on:
 - Quality of report
 - Performance (speed/delay)
 - Power dissipation
 - Layout area
- ❑ There will be a 10% extra credit for any design with minimum layout area, or maximum performance, or minimum power consumption

Course Objectives

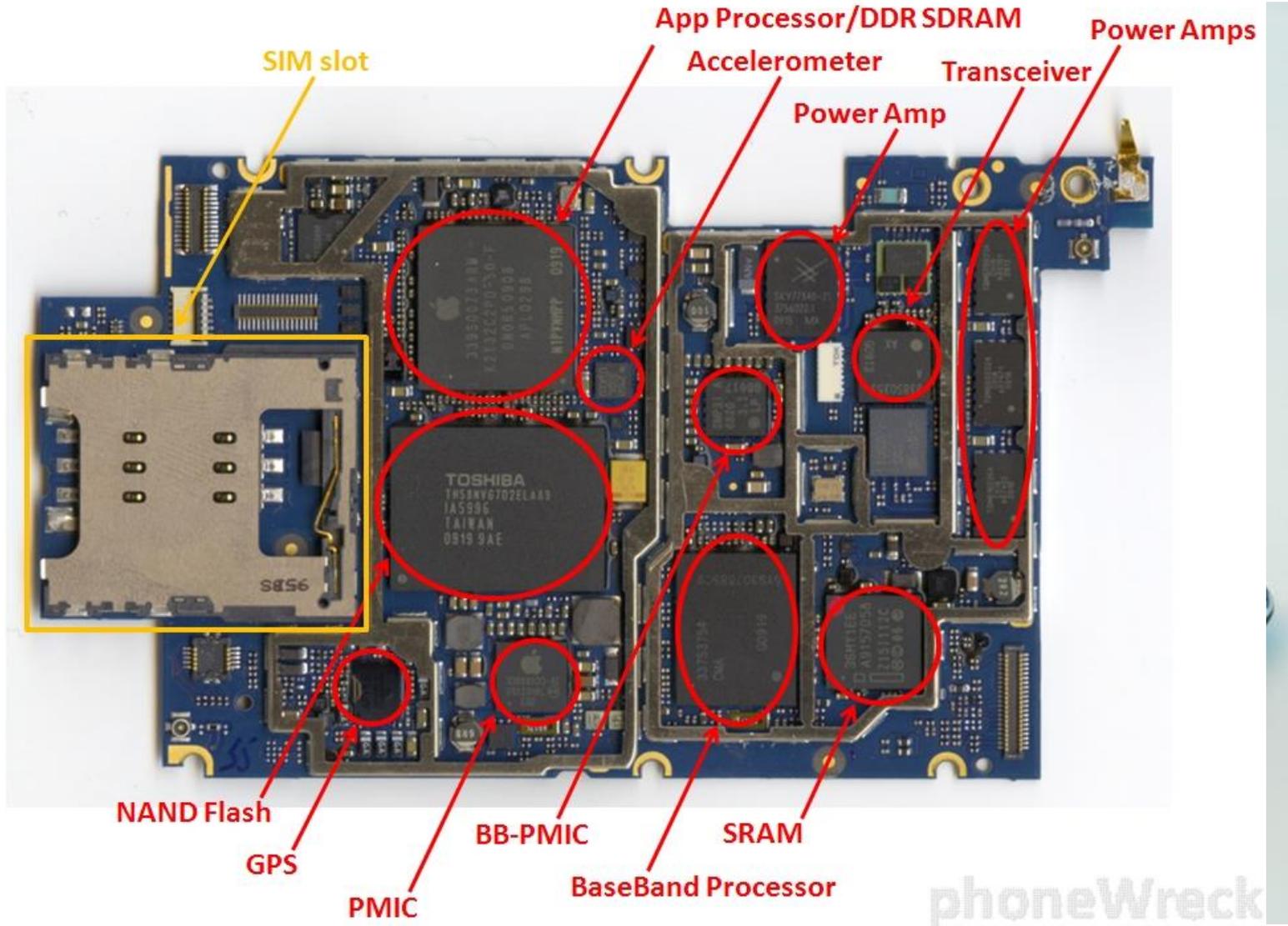
- Analyze the basic device physics and predict the behavior of electrons and holes in a p-n junction
- Analyze multiple diode circuits with different types of diodes using the piecewise linear model and the small-signal equivalent circuit
- Analyze the operation of a field effect transistor and determine the DC/AC response of the FET
- Design and analyze the operation of the CMOS Inverter, NAND, NOR, and T-gates
- Determine the layout diagram for various logic gates
- Draw the fabrication steps for fabrication of logic gate circuits
- Understanding the concept of timing analysis, delay, and power estimations

Class Schedule

Warning: Lecture schedule subject to change!!

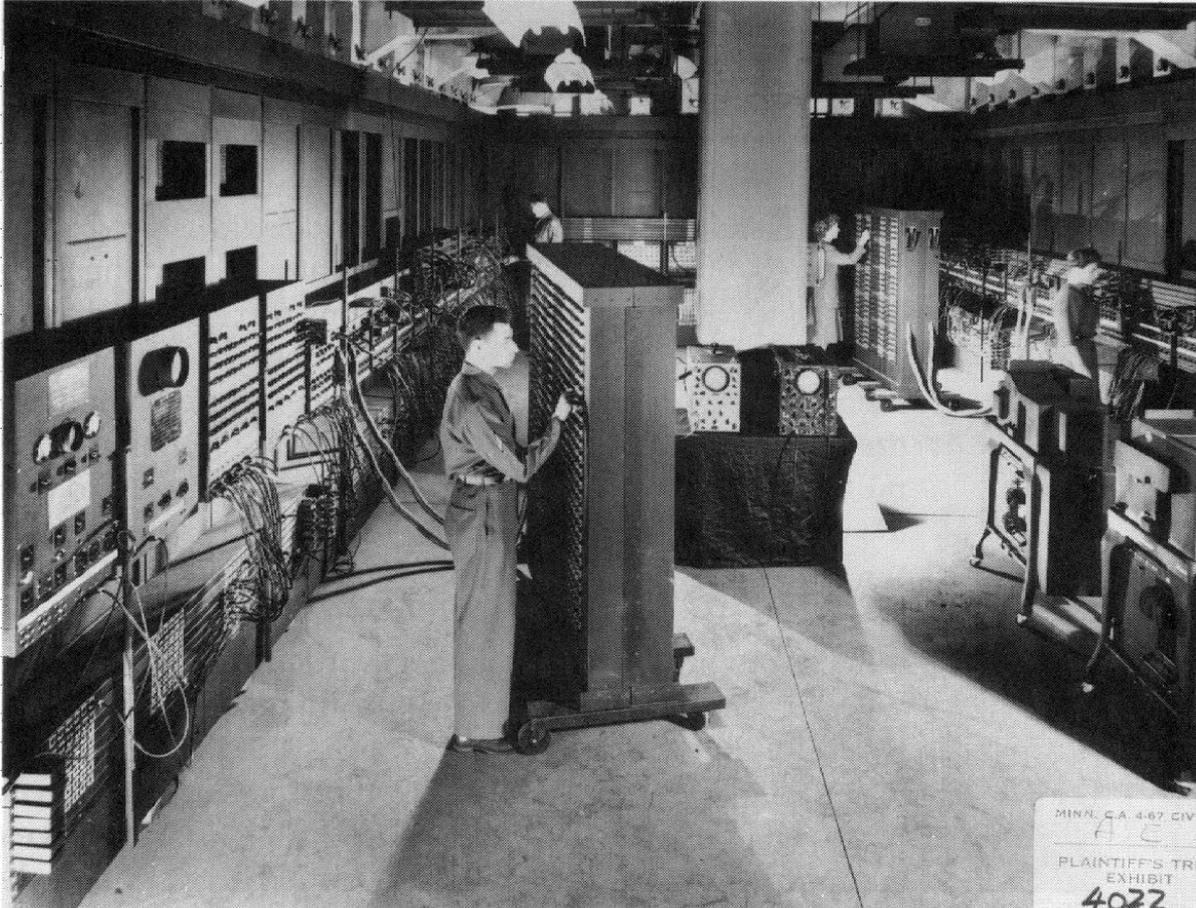
Date	Day	Topic	Reading/Coverage
August 18	Mon	Introduction to Digital Electronics	Handout
August 20	Wed	Basic Circuits with Diodes	1.1 - 1.8
August 25	Mon	Basic Solid State Physics	2.1 - 2.3
August 27	Wed	Physics of Semiconductor Diodes	2.4 - 2.6
September 1	Mon	Labor Day	-
September 3	Wed	PSPICE Review	Handout
September 8	Mon	Physics of Semiconductor MOSFETs	3.1
September 10	Wed	MOSFET I-V Characteristics	3.2
September 15	Mon	Basic Circuits with MOSFET	Handout
September 17	Wed	MOSFET Threshold Voltage & Parasitic Capacitance	Handout
September 22	Mon	MOSFET Scaling Issues	Handout
September 24	Wed	Basic Digital Circuits with MOSFETs	Handout
September 29	Mon	CMOS Inverter VTC & ITC	5.1 - 5.4
October 1	Wed	Midterm Exam #1	-
October 6	Mon	CMOS Inverter Noise Margin & Delay Model	5.5
October 8	Wed	CMOS Inverter Power	5.6
October 13	Mon	CMOS Inverter Short Circuit Power	5.6
October 15	Wed	CMOS Inverter Leakage Power	5.7
October 20	Mon	Gate Sizing (Inverter Chain)	5.8
October 22	Wed	Interconnect Modeling I	4.1 - 4.2
October 27	Mon	Interconnect Modeling II	4.3 - 4.4
October 29	Wed	CMOS Fabrication	12.1 - 12.9
November 3	Mon	Design Rules & Basic Layout Techniques	11.1 - 11.6
November 5	Wed	Midterm Exam #2	-
November 10	Mon	Combinational Logic: NAND & NOR Gates	6.1 - 6.2
November 12	Wed	Combinational Logic: Transmission Gates	6.3
November 17	Mon	Logic Design Style: Static Logic	7.1
November 19	Wed	Logic Design Style: Dynamic & Domino Logics	7.2 - 7.3
November 24	Mon	Sequential Logic: D Flip-Flop	8.1 - 8.4
November 26	Wed	Timing Analysis	8.9
December 1	Mon	SRAM Memories	9.1 - 9.3
December 3	Wed	DRAM & FLASH Memories	9.4 - 9.6
December 8	Mon	Final Exam (5:30-7:30PM)	-

Example of a Digital Integrated Circuit?



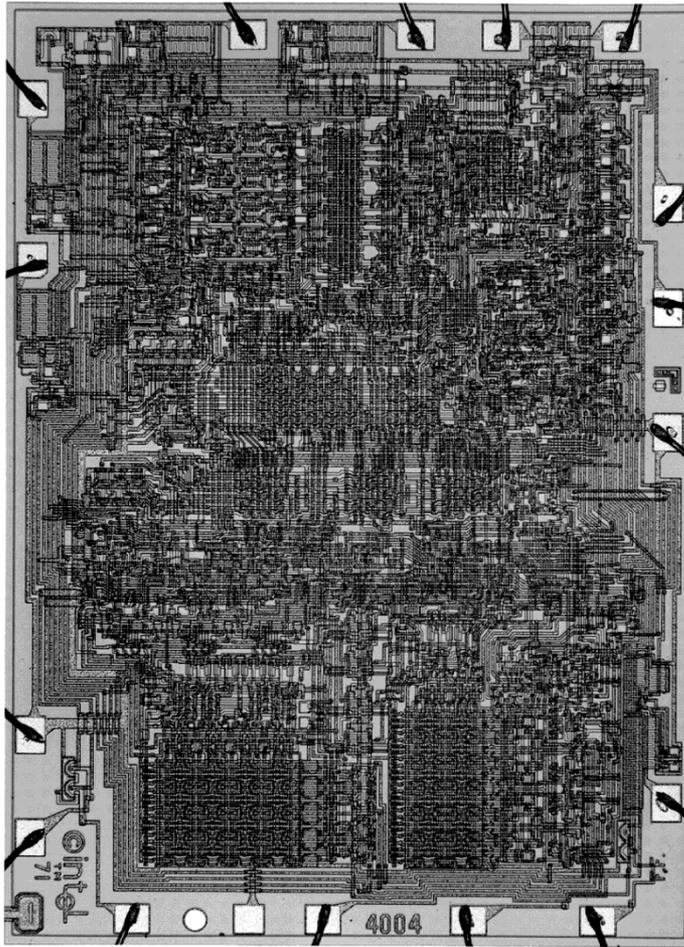
Introduction

Beginning of the Computer: ENIAC, the first electronic computer (1946)



- 333 integer multiplication/second
- A six-week run was equivalent to 100 person-years of manual computation
- Program resides in the wired connections

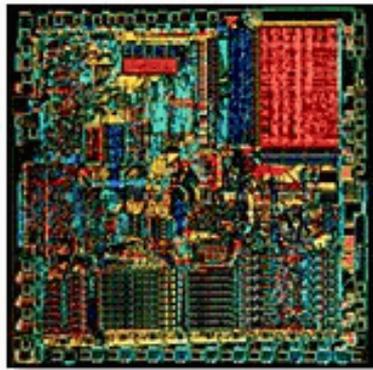
Intel 4004 Microprocessor



- 1971
- 10 um NMOS-only
- 2300 transistors
- 1 MHz

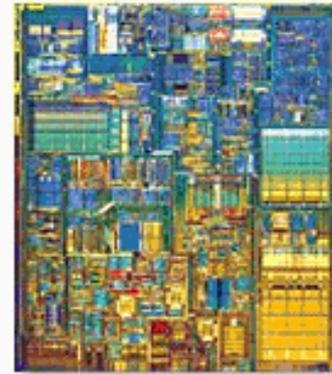
Intel Technology Advancement

Processor Comparison



Intel® i8088

Year: 1981
29,000 transistors



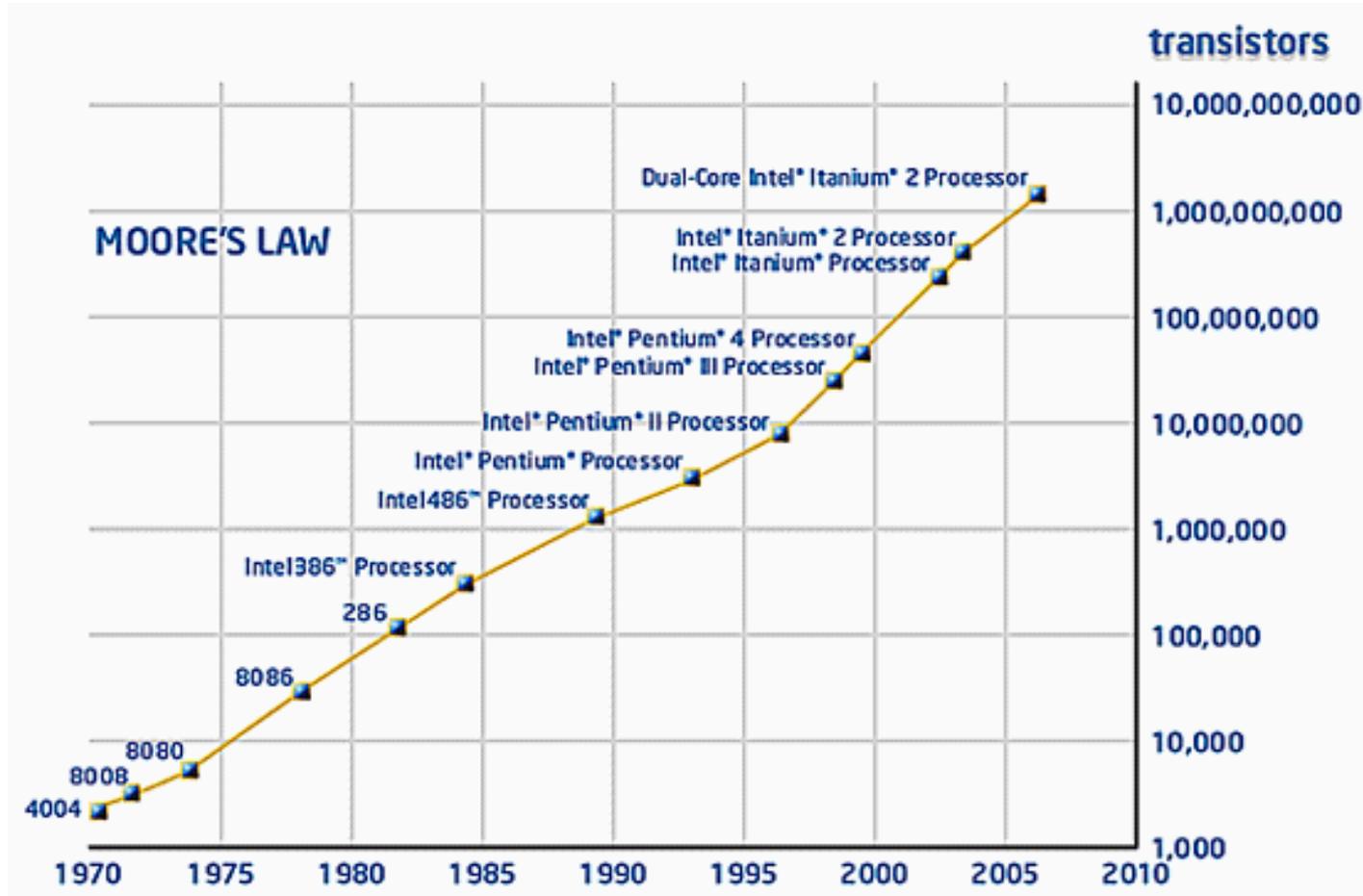
**Intel® Pentium® 4 Processor
with HT Technology**

Year: 2004
125,000,000 transistors

Moore's Law

- ❑ In 1965, Gordon Moore (founder of Intel) had a very interesting observation. He noticed that the number of transistors on a chip doubled every 18 to 24 months.
- ❑ He made a prediction that semiconductor technology would double its effectiveness every two years.

Moore's Law for Intel Microprocessors



Source: www.intel.com

Moore's Law in Travel Industry



1978

Approximate Cost: **\$900**

Approximate Travel Time: **7 hours**

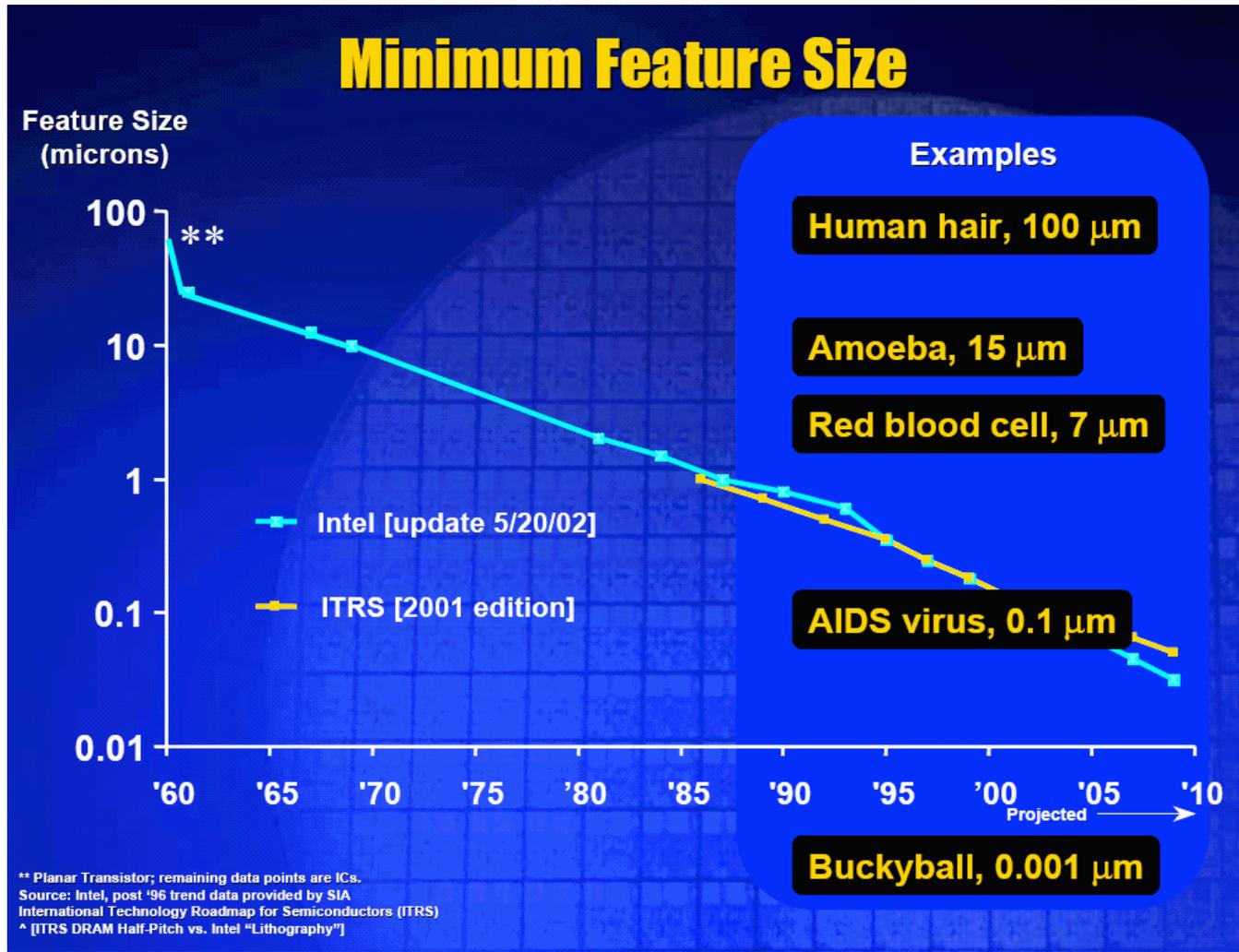


2003

Approximate Cost: **1¢**

Approximate Travel Time: **1/4 second**

CMOS Scaling Scenario

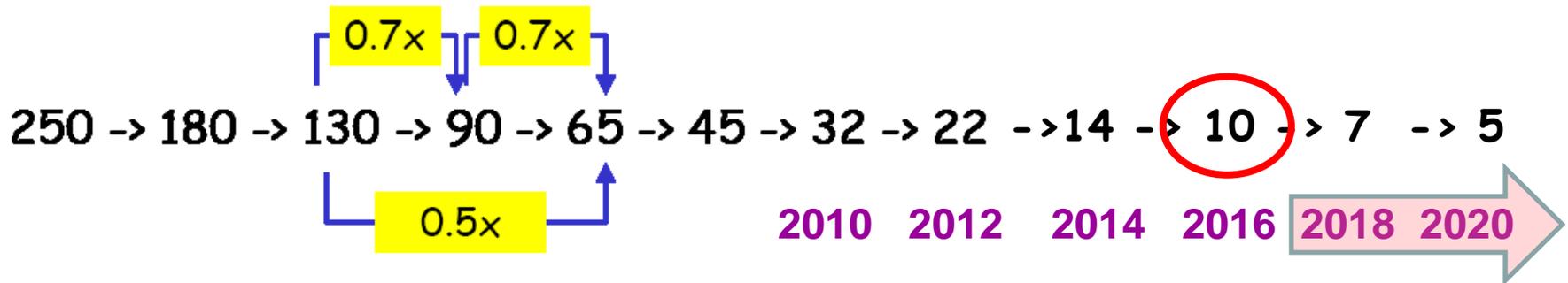


Why Scaling?

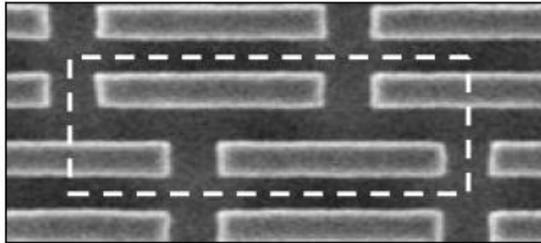
- ❑ **What are the benefits of technology scaling?**
- ❑ **Why smaller device is better?**

CMOS Scaling Calculation

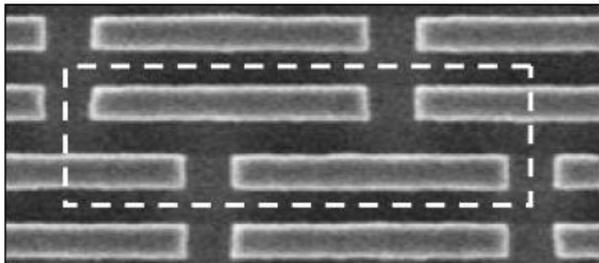
Scaling Calculator



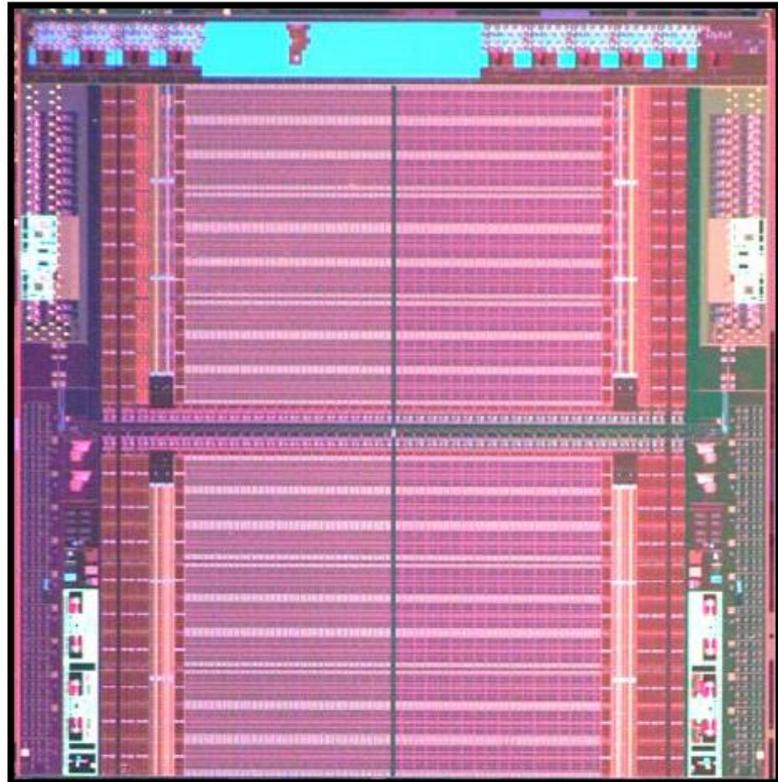
22nm SRAM Testchip (Intel)



0.092 μm^2 SRAM cell
for high density applications

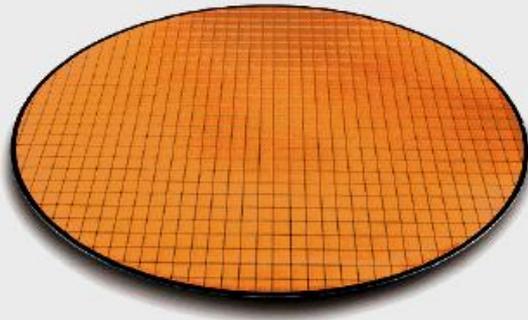
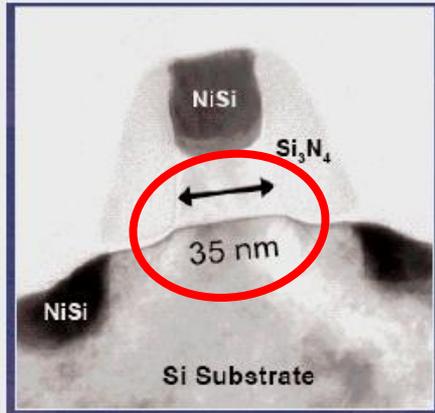


0.108 μm^2 SRAM cell
for low voltage applications



**10 million of these cells could fit in a square millimeter
– about the size of the tip of a ballpoint pen**

MOS in 65nm of Core Duo Processor



Intel strained silicon (top) and a 65-nm wafer of Intel® Core™ Duo processors (bottom).

Distance between Si atoms = 0.357 nm

No. of atoms in channel = $35 \text{ nm} / 0.543 \text{ nm}$
= 64 Atoms!

Problem: Uncertainty in transistor behavior and difficult to control variation!

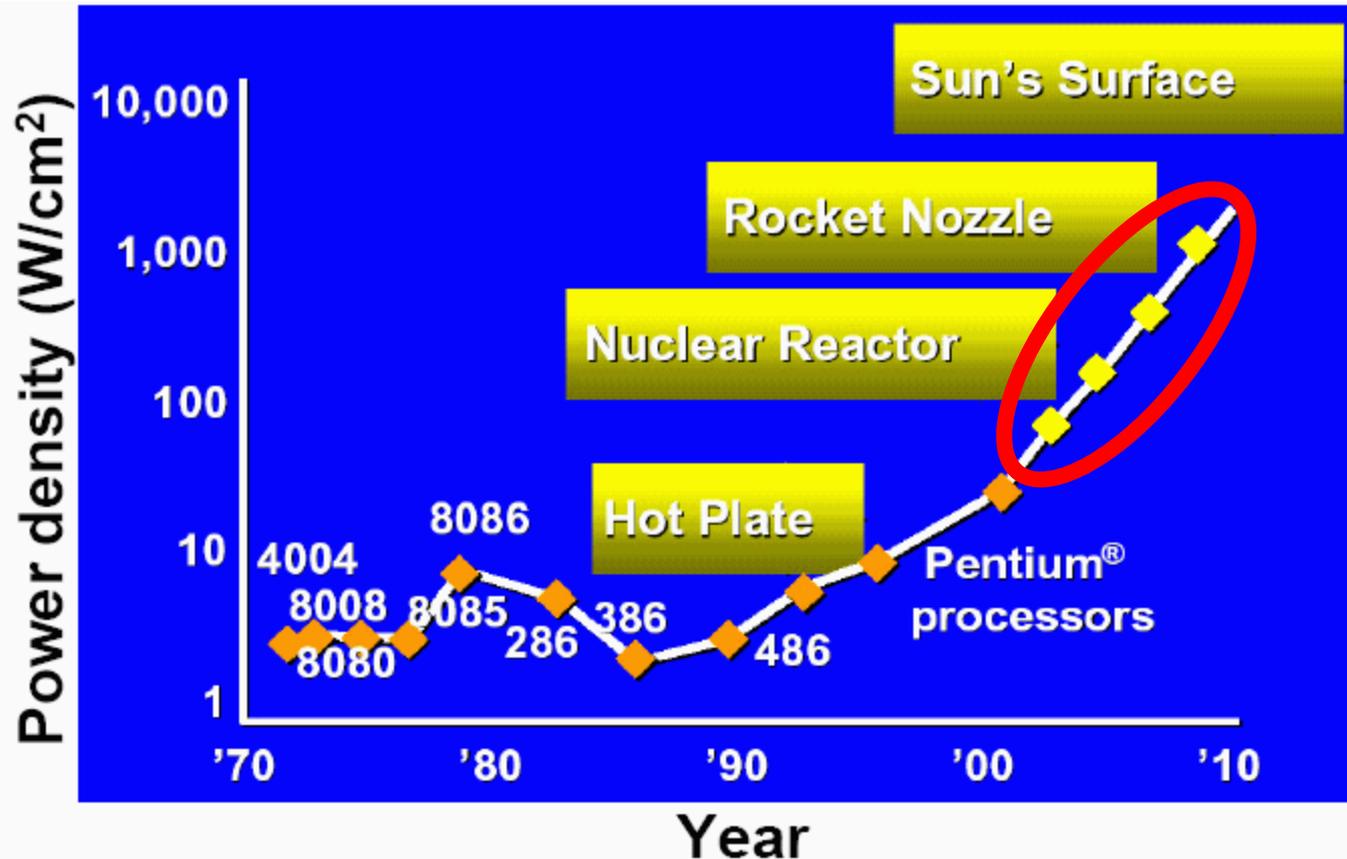
Benefit of Smaller Transistors

- 1) More transistors in the same foot-print**
- 2) More functionality**
- 3) Reduced cost per function**
- 4) Faster devices and higher performance**
- 5) Lower switching energy per transistor**

Transistor Scaling Challenges

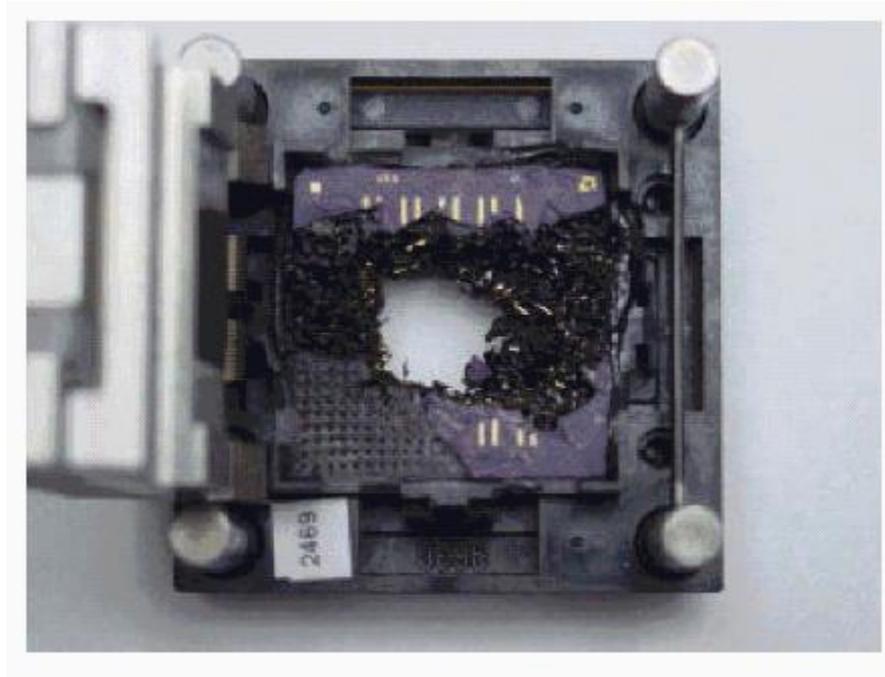
- 1) Feature sizes down to few atomic layers**
- 2) Increase uncertainty of transistor behavior**
- 3) Increase leakage power consumption**
- 4) Difficult to maintain performance enhancement**
- 5) Thermal limit issue**

Power Density Problem

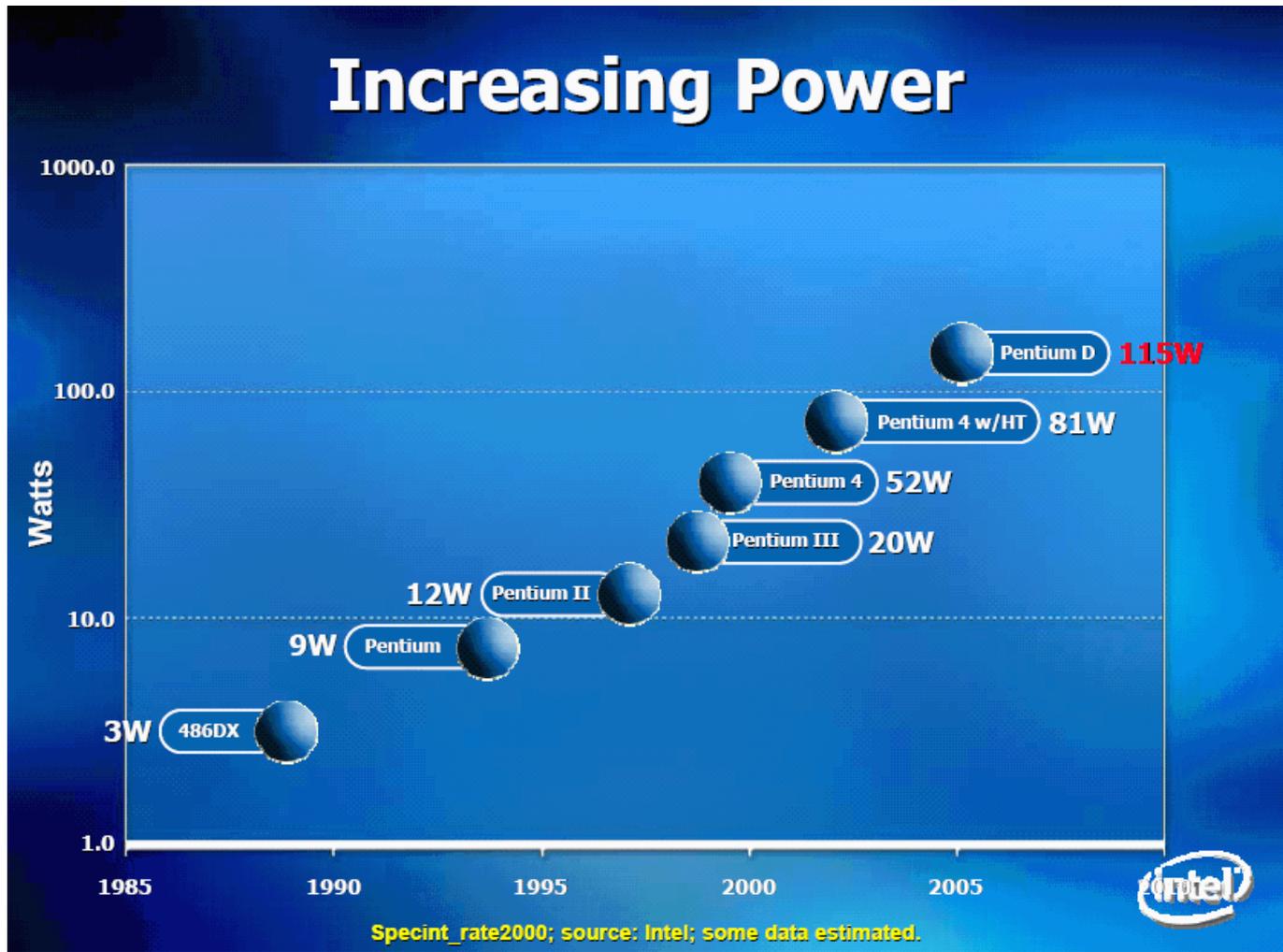


***Power density too high to keep junction at low temperature.
Power reaching limits of air cooling.***

Heat Management Consideration



Power Consumption Scenario



Some Calculations!

Power = 115 Watts

Supply Voltage = 1.2 V

Supply Current = $115 \text{ W} / 1.2 \text{ V} = 96 \text{ Amps!}$

Problem: Current density becomes a serious problem!

This is known as electromigration

Note: Fuses used for household appliances = 15 to 40 Amps

Another Calculations!

Power = 115 Watts

Chip Area = 2.2 Cm²

Heat Flux = 115 W / 2.2 Cm² = 50 W/Cm² !

Problem: Heat flux is another serious issue!

Notes:

Heat flux in iron = 0.2 W/Cm²

Heat flux in frying pan = 10 W/Cm²

Method of Heat Management

- 1) Proper heat removal system (expensive)**
- 2) Improve manufacturing for low power MOS**
- 3) Architectural solutions (multi-cores)**

Hitachi Water Cooling Laptop



Summary

Digital IC Business is Unique

Things Get Better Every Few Years

Companies Have to Stay on Moore's Law Curve to Survive

Benefits of Transistor Scaling

Higher Frequencies of Operation

Massive Functional Units, Increasing On-Die Memory

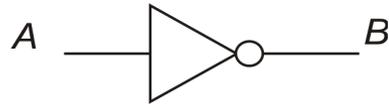
Cost/Functionality Going Down

Downside of Transistor Scaling

Power (Dynamic and Static)

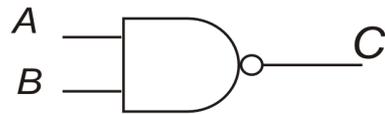
Design and Manufacturing Cost

Basic Logic Gates



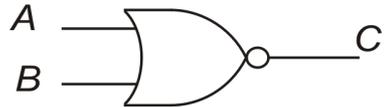
A	B
1	0
0	1

Inverter



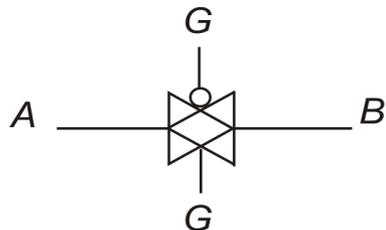
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

NAND



A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

NOR



A	G	B
1	1	1
0	1	0
1	0	Z
0	0	Z

Transmission Gate

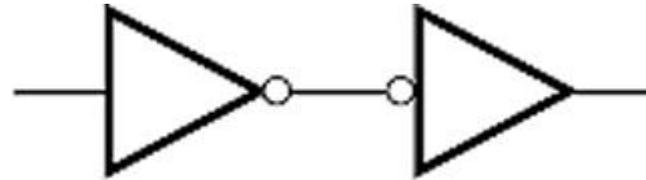
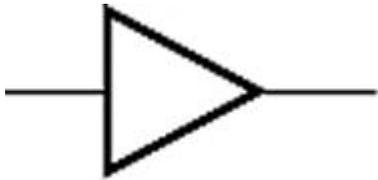
Review: DeMorgan's Theorem

1. Product terms (AND) in the original function transform to sum (OR) terms in the DeMorgan equivalence.
2. Sum (OR) terms in the original function transform to product (AND) terms in the DeMorgan equivalence.
3. All variables are inverted when transforming to and from a DeMorgan equivalence.
4. An overbar on the original function transforms to no overbar in the DeMorgan equivalence, and vice versa.

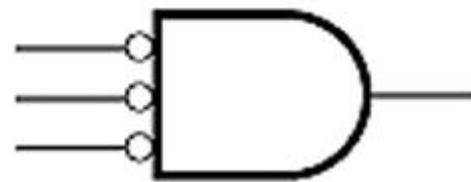
$$\overline{X + Y} = \overline{X} \overline{Y}$$

$$\overline{XY} = \overline{X} + \overline{Y}$$

Alternative Gate Representation



Buffer

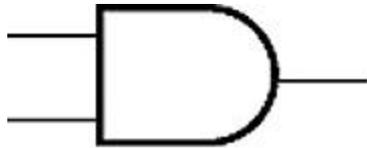


3-input NOR



3-input NAND

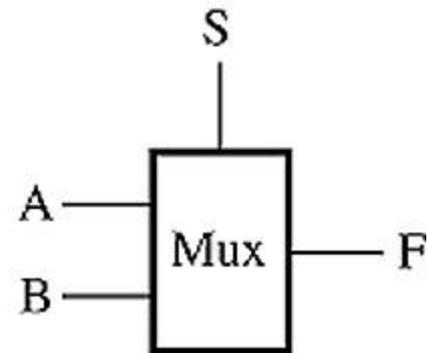
Example 1: Use Basic Gates to Create Each



AND



XOR



OR



XNOR

Basic Boolean Properties

$$X + Y = Y + X$$

$$X + 0 = X$$

$$X0 = 0$$

$$X + X = X$$

$$X\bar{X} = 0$$

$$(X + Y) + Z = X + (Y + Z)$$

$$X(Y + Z) = XY + XZ$$

$$\overline{X + Y} = \bar{X}\bar{Y}$$

$$XY = YX$$

$$X + 1 = 1$$

$$X1 = X$$

$$XX = X$$

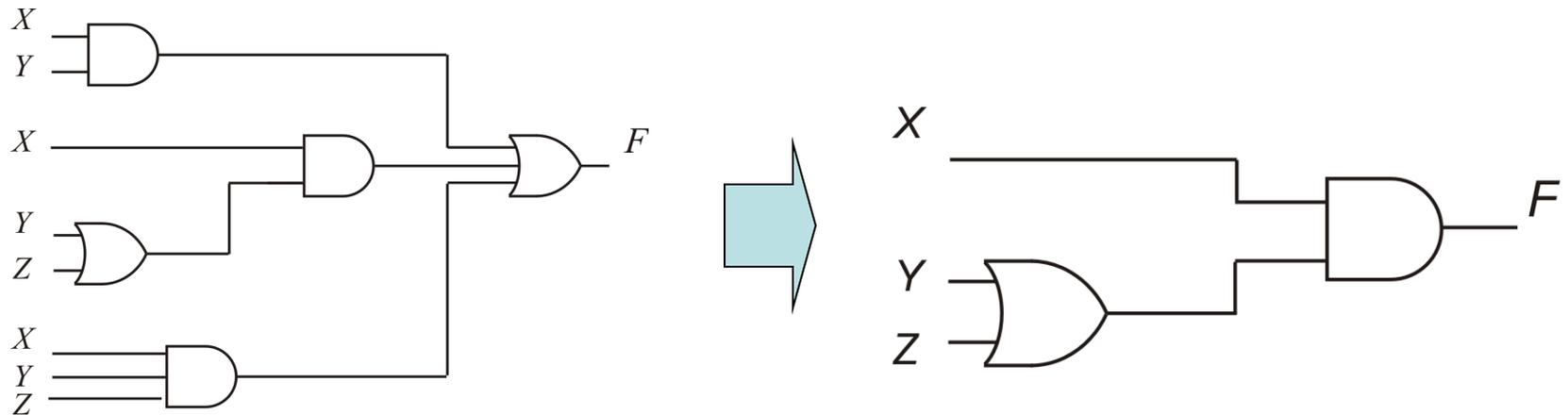
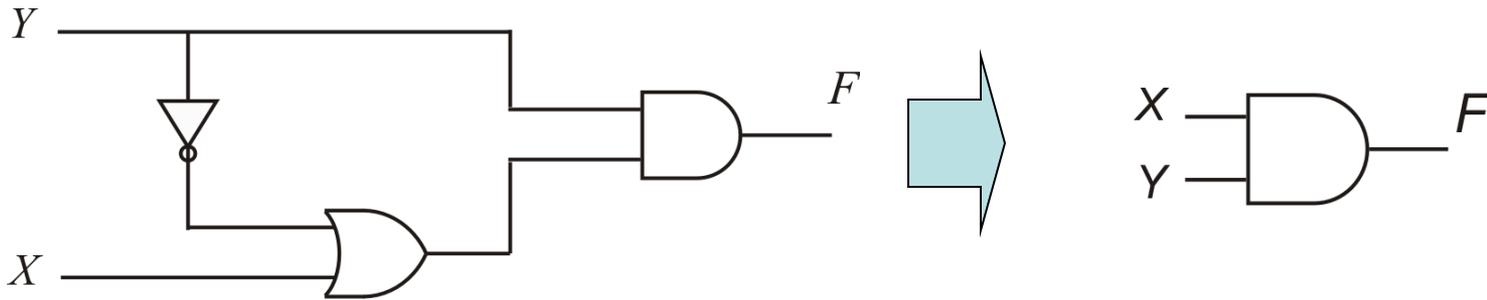
$$X + \bar{X} = 1$$

$$(XY)Z = X(YZ)$$

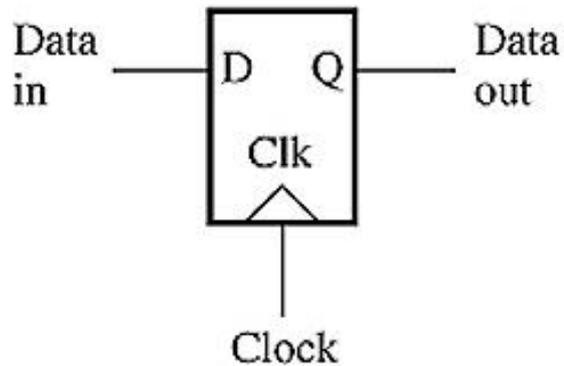
$$X + (YZ) = (X + Y)(X + Z)$$

$$\overline{XY} = \bar{X} + \bar{Y}$$

Example 2: Reduce to the Minimum Gates



Positive Edge D Flip-Flop

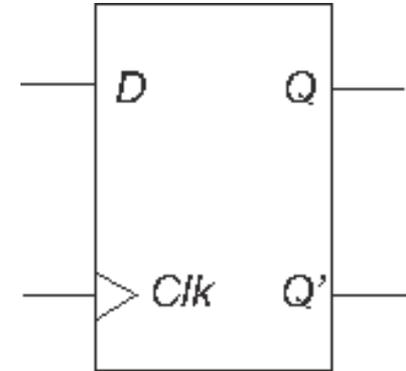
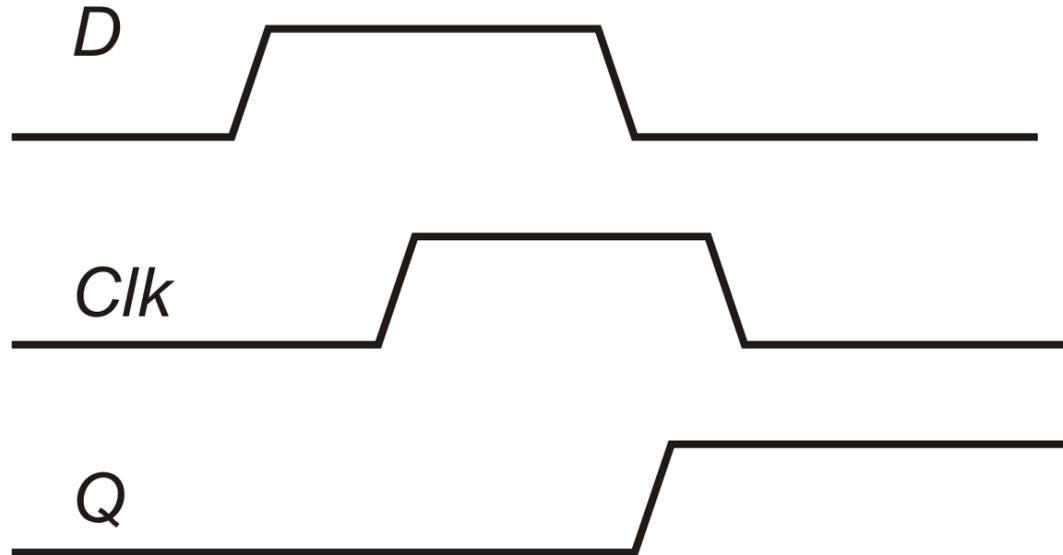


DFF schematic

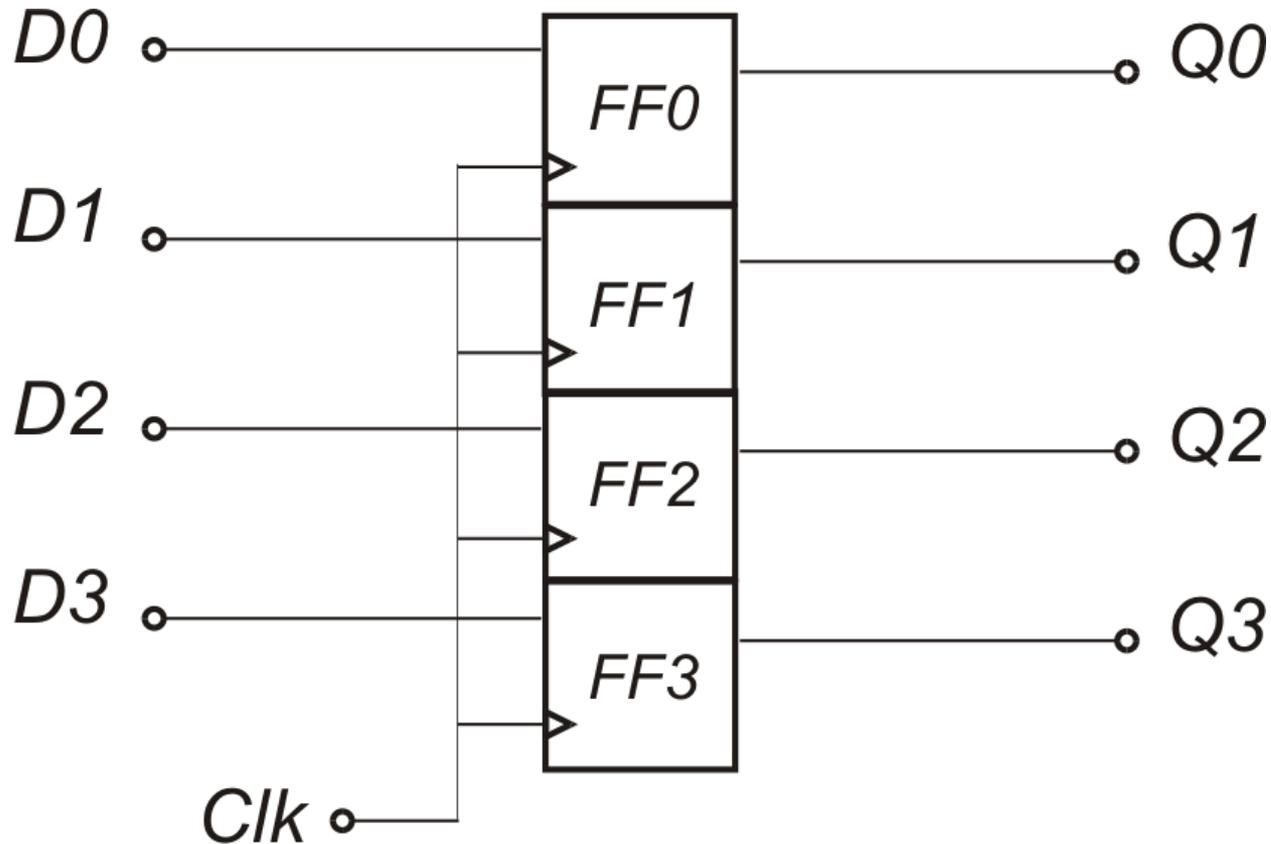
Clk	D	Q (old)	Q (new)
0	X	0	0
0	X	1	1
0 → 1	0	X	0
0 → 1	1	X	1
1	X	0	0
1	X	1	1
1 → 0	X	0	0
1 → 0	X	1	1

Excitation table

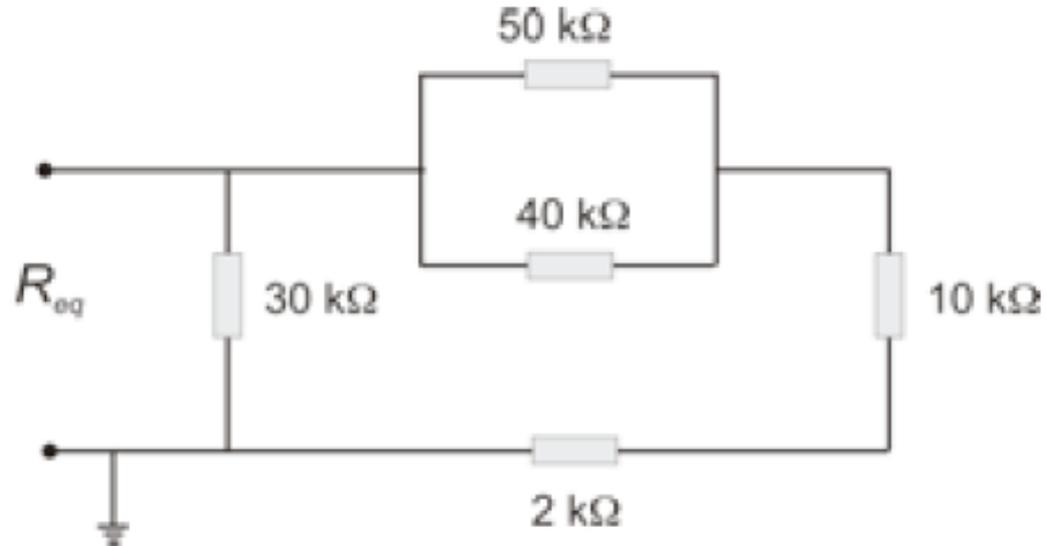
Timing in a D Flip-Flop



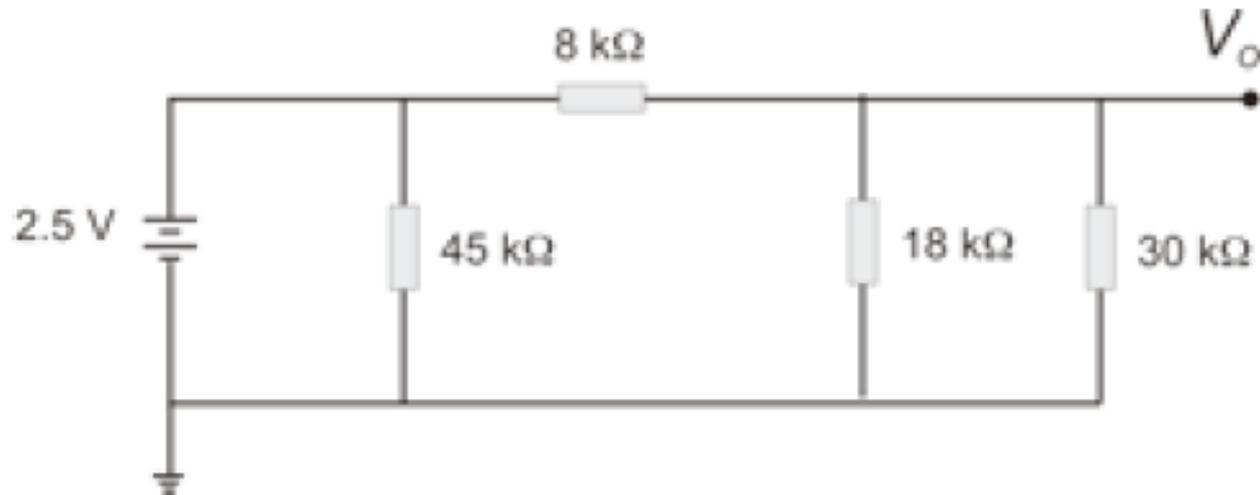
4-bit Register using D Flip-Flop



Review: Circuit Analysis – Find R_{eq}



Review: Circuit Analysis – Thevenin Circuit



Review: Circuit Analysis – Power Calculation

